MOHAMMAD MONJUR

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EDUCATION

University of New Hampshire, New Hampshire *Expected: May 2025*
Ph.D in Electrical and Computer Eng. specialization on "Hardware Security and Trust" *GPA:4.0*
Coursework: Hardware Security and Trust I, Hardware Security and Trust II.
University of New Hampshire, New Hampshire *Aug 2020*
M.Sc in Electrical and Computer Eng. specialization on "Hardware Security and Trust" *GPA: 3.8*
Coursework: Robust IC, Cyber Security, Computer Security, VLSI Circuit Design, Appl. of Integrated Circuits.

SKILL SETS

Application Specific Integrated Circuits

- Complete ASIC design flow using Verilog and EDA/CAD Tools.
- Functional Verification, Logic Synthesis, Place-and-Route and Static Timing Analysis.

Computer Architecture

- In-depth understanding of security analysis and performance evaluation for embedded architecture.

Languages Verilog, C/C++, Python, Bash, x86 assembly
Tools Cadence Virtuoso, Cadence NCSim, MATLAB, LTspice and Multisim
Hardware FPGA Boards (NEXYS A7), MCU Boards (Raspberry Pi 4, Arduino MKR WAN 1300), Scanning Electron and Microscope (ZEISS Ultra 55), Atomic Force Microscope (Veeco D5000-1)

INDUSTRIAL EXPERIENCE

University of New Hampshire InterOperability Laboratory May 2024 - Current
Embase Engineer *Durham, NH*

- Led developer of sub-nanosecond synchronization systems for advanced distributed networks using White Rabbit, enhancing precision timing for high-energy physics, fusion research, and quantum networking.
- Collaborated with research institutions and industrial partners to validate and measure timing solutions, ensuring compatibility and accuracy in time-sensitive telecommunications and cyber-physical systems.
- Provided technical resources and guidance to expand the White Rabbit open-source ecosystem, enabling community-driven innovation and supporting advanced manufacturing and large distributed databases.
- Performed system calibration and performance assessments to optimize synchronization accuracy, leveraging White Rabbit for applications in deterministic networks and real-time data processing.

Advanced Micro Devices Inc June 2012 – April 2013
Failure Analysis Engineer *Singapore*

- Designed sample preparation (Backside De-processing and laser voltage probing method) for PS4 and Xbox1 CPU device under test (DUT).
- Experienced in preparing semiconductor samples for Laser Voltage Probing to identify electrical faults in integrated circuits using advanced flip-chip technology.
- Conduct thermal stress testing to observe coefficient of thermal expansion between silicon chip and packaging.
- Experienced with Laser Scanning Injection Microscopy (LSIM), utilizing laser-induced techniques to inject charge into semiconductor devices to identify faulty transistors.
- Improved electrical characterization of contact level PVC (Passive Voltage Contrast) using Scanning Electron Microscopy (SEM) and fault localization on semiconductor circuits.
- Experienced in employing Atomic Force Microscopy to measure surface roughness at the nanometer scale to ensure surface material quality and consistency.
- Used focused ion beam (FIB) for precise device modification, circuit editing, and material deposition, essential for customizing semiconductor components and rapid prototyping.

RESEARCH PROJECT

University of New Hampshire Aug 2018 - Present

- Developed a novel detection system with 100% to identify and mitigate malicious activities in hardware devices, utilizing the continuous time convolution method to maintain reliability of LoRaWANs protocols.

- Designed and implemented a Finite State Machine (FSM) achieving 100% test coverage, significantly enhancing reliability and security against hardware Trojan attacks.
- Developed a hybrid convolutional-recurrent neural network architecture can handle multi-label classification with 44% fewer neurons than RNN and 12% higher sensitivity in identifying attacks than CNN. Implemented differential power analysis attack on cryptographic operation (logic-locked circuits) to leak key using statistical analysis and error correction of power traces with 67.67%
- Implemented digital ASIC design flow consisting of RTL design, verification, synthesis, physical design, timing analysis, and code coverage analysis to perform low-switching nets in design to reduce power consumption.
- Implemented an arbiter-based physical unclonable function to analyze the improve uniformity from 50% to 77.78% for cryptography key.
- Developed input integrity checks and exclusive logic-based attack detection methods to address attacks on approximate computing systems with an area of 6.8% and power overhead of 1.5% less.
- Implemented I^2C protocol in cadence design system to implement the analog circuits to mitigate clock mute attack with a success rate of over 98%.

Advanced Micro Devices Inc June 2012 – April 2013

- Thermal effect on die warpage during back-side die polishing of flip-chip ball grid array (BGA) device.
- Evaluated equipment for sample preparation and electrical fault isolation by laser voltage probing (LVP) and developed standardized testing procedures within the organization.

SCIENTIFIC CONTRIBUTIONS

- Mohammad Monjur and Qiaoyan Yu. 2024. CTC: Continuous-Time Convolution Based Multi-Attack Detection for Sensor Networks. In 2024 IEEE International Symposium on Circuits and Systems (ISCAS).
- N. C., Mohammad Monjur, W. Lu and Q. Yu "A Hybrid Neural Network for Simultaneous Multi-Attack Detection in Sensor Networks." AsianHOST, Tianjin, China, 2023.
- Kajol, M.A.; Monjur, M.M.R.; Yu, Q. "A Circuit-Level Solution for Secure Temperature Sensor." Sensors 2023, 23, 5685
- Mohammad Monjur, J. C., M. Kajol, and Q. Yu, "Hardware Security in Advanced Manufacturing." In Proceedings of the Great Lakes Symposium on VLSI 2022.
- M. Monjur, J. Heacock, J. C., R. Sun and Q. Yu, "Challenges of Securing Low-Power LoRaWAN Devices Deployed in Advanced Manufacturing," 23rd ISQED, Santa Clara, CA, USA, 2022.
- M. M. R. Monjur, J. Heacock, R. Sun and Q. Yu, "An Attack Analysis Framework for LoRaWAN Applied Advanced Manufacturing" 2021 Virtual IEEE HST.
- M. R. Monjur, S. Sunkavilli and Q. Yu, "ADobf: Obfuscated Detection Method against Analog Trojans on I^2C Master-Slave Interface," 2020 IEEE 63rd International MWSCAS.
- P. Yellu, M. R. Monjur, T. Kammerer, D. Xu and Q. Yu, "Security Threats and Countermeasures for Approximate Arithmetic Computing," 25th ASP-DAC, 2020.
- P. Yellu, Z. Zhang, M. M. R. Monjur, R. Abeysinghe and Q. Yu, "Emerging Applications of 3D Integration and Approximate Computing in High-Performance Computing Systems: Unique Security Vulnerabilities," 2019 IEEE High Performance Extreme Computing Conference.
- Monjur, M.M.R.; Wei, M.S.; Chong, H.B.; Nasar-Abdat, L.; Narang, V., "Thermal effect on die warpage during back-side die polishing of flip-chip BGA device," 20th IEEE IPFA 2013.

OUTREACH PROGRAM

- Demonstrated hardware security projects to students of Oyster High School as Part of a K-12 outreach program from NHCyberSEE Lab at Kingsbury Hall Dec. 2023.
- Organized "Cyber Security" workshop at UNH to bring together industrial expertise, Oct. 2022.
- Organized "Women in Hardware and Systems Security Workshop" workshops at UNH aims to attract more women to join the hardware and systems security, Oct. 2022.
- OISS Orientation leader to assist new international students for Fall'22.

AWARDS, HONORS & SCHOLARSHIPS

- Awarded **Research Assistantship** for academic and research excellence Dept. of ECE, UNH since Fall'22.
- Second placed winner in "Hackathon/Ideathon Event" at ECenter - how to increase the growth of the Ski Industry/Diversity in New Hampshire (October 23, 2021).
- Awarded **Teaching Assistantship** for academic and research excellence Dept. of ECE, UNH (Spring 2019 to Spring 2022).
- Finalist of CSAW'18 Embedded Security Challenge, the largest cybersecurity event.
- Recipient of **CEPS-Industry scholarships** in Fall 2018 on merit basis Fellowship, UNH.