Clause 40

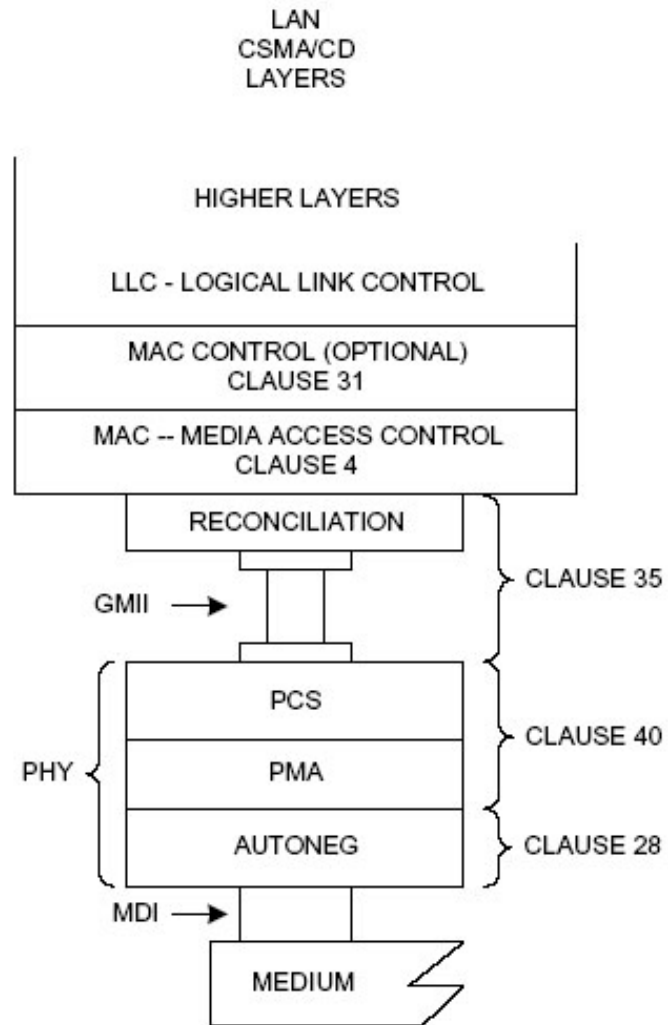## 1000BASE-T Physical Medium Attachment (PMA) Sublayer

Presentation Overview:

- Location in the OSI stack

- Interface with PCS

- Interface with Auto-Negotiation

- PAM-5 Encoding Scheme

- PMA Sublayers Functionality and Functions

- PMA Electrical Specifications

PMA in the OSI Model

LAN
CSMA/CD
LAYERS

HIGHER LAYERS

LLC - LOGICAL LINK CONTROL

MAC CONTROL (OPTIONAL)
CLAUSE 31

MAC -- MEDIA ACCESS CONTROL
CLAUSE 4

RECONCILIATION

GMII →

CLAUSE 35

PCS

CLAUSE 40

PHY { PMA

AUTONEG

CLAUSE 28

MDI →

MEDIUM

OSI: PCS

- Transmits 8-bit code groups in parallel at 125 MHz for the PMA to serialize

- Translates the data to be sent into a suitable form.

- The PCS operating functions are:
  - PCS Transmit Enable, PCS Transmit, PCS Receive, and PCS Carrier Sense

- PCS passes the 4D 5 level (+2, +1, 0, -1, -2) coding to the PMA to convert to electrical signaling

OSI: PMA (General Role)

• The PMA is the interface between the PCS and Auto-negotiation

• Primary role is to Serialize and De-serialize the incoming data stream coming to and from the MDI

• Implements PAM-5 (Voltage dependant signaling between MDI/PMA)

• Controls Partial Response

OSI: PCS/PMA

- – Shown here is the basic interface between the PCS and PMA

- – The PCS takes in 8 bits of parallel data and sends the PMA 4, "5 level symbols" which can take on the values shown

- – The PMA adds partial response and converts the quinary symbols to PAM-5 signaling to interface with the MDI, taking on the values shown

5 Voltage levels
[-1, -1/2, 0, +1/2, +1]

8- Bits

PCS

PMA

4 - 5 level Symbols
[-2, -1, 0, +1, +2]
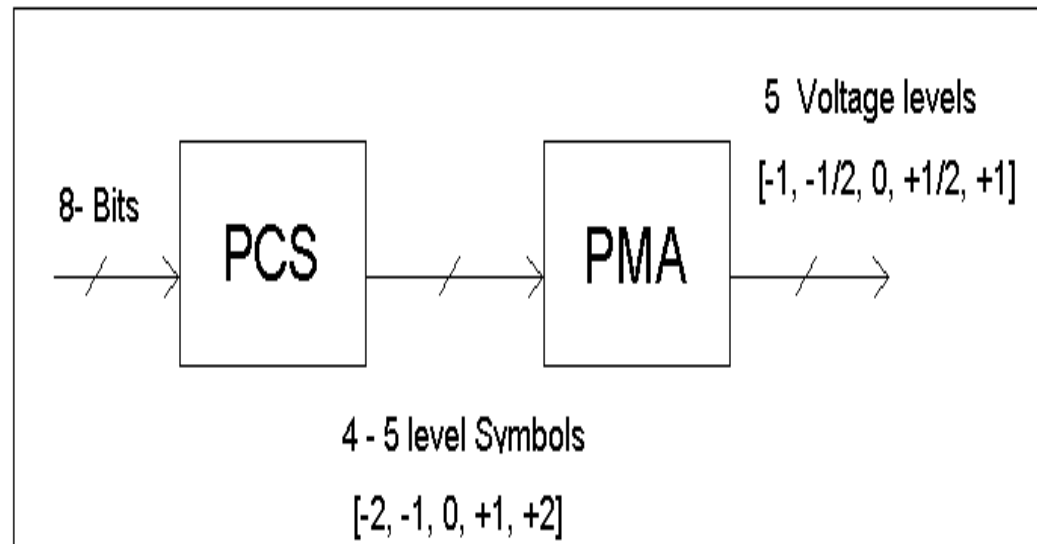
OSI: Auto-Negotiation

- Required for 1000Base-T Operation

- Advertise Abilities

    - Transmission speeds

    - Half and/or Full Duplex

- Determine Master and Slave relationship

    - Uses prioritization scheme

    - Base page, Next page, etc... To establish fast possible link (1000Mb/s)

- Needed for PHY Control, a PMA subfunction

OSI: MDI/MDI-X

• Medium Dependant Interface

• MDI is specified as the mechanical interface to the balanced cabling for 1000Base-T Ethernet

Table 40–12—Assignment of PMA signal to MDI and MDI-X pin-outs

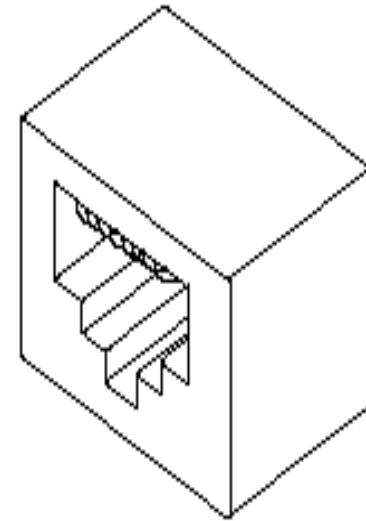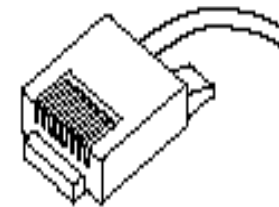| Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA−	BI_DB−
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC−	BI_DD−
6	BI_DB−	BI_DA−
7	BI_DD+	BI_DC+
8	BI_DD−	BI_DC−

Figure 40–29—MDI connector

PIN 1

Figure 40–30—Balanced cabling connector

OSI: Automatic MDI/MDI-X

- Purpose (optional)
  - The main role of the Automatic MDI/MDI-X is to eliminate the need for using crossover cables
  - Able to randomly switch between MDI and MDI-X configuration after listening for Fast Link Pulses (FLPs) for a specified amount of time (62 ±2 ms)

PAM-5 and Partial Response

- The MDI and PMA use a modulation scheme over each pair which is called, 5-level Pulse Amplitude Modulation (PAM-5)

- PAM5 signaling
  - Five discrete voltage levels [-1, -½, 0, +½, +1] volts
  - Lowers signaling bandwidth
  - Allows for 2 bits per symbol
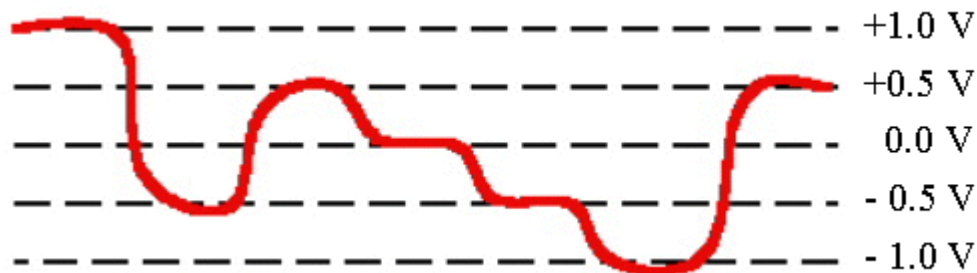
PAM-5 and Partial Response

- The PAM-5 Implementation is intrinsic in achieving 1000Mb/s

    - 125 MHz signaling rate   = 125
        (As proven over CAT-5 by 100Base-TX)
    - Using PAM-5 @ 2 bits per symbol   =   x 2
    - Use all 4 pairs of CAT 5 cable   =   x 4
    - Results in: 1000 Mb/s
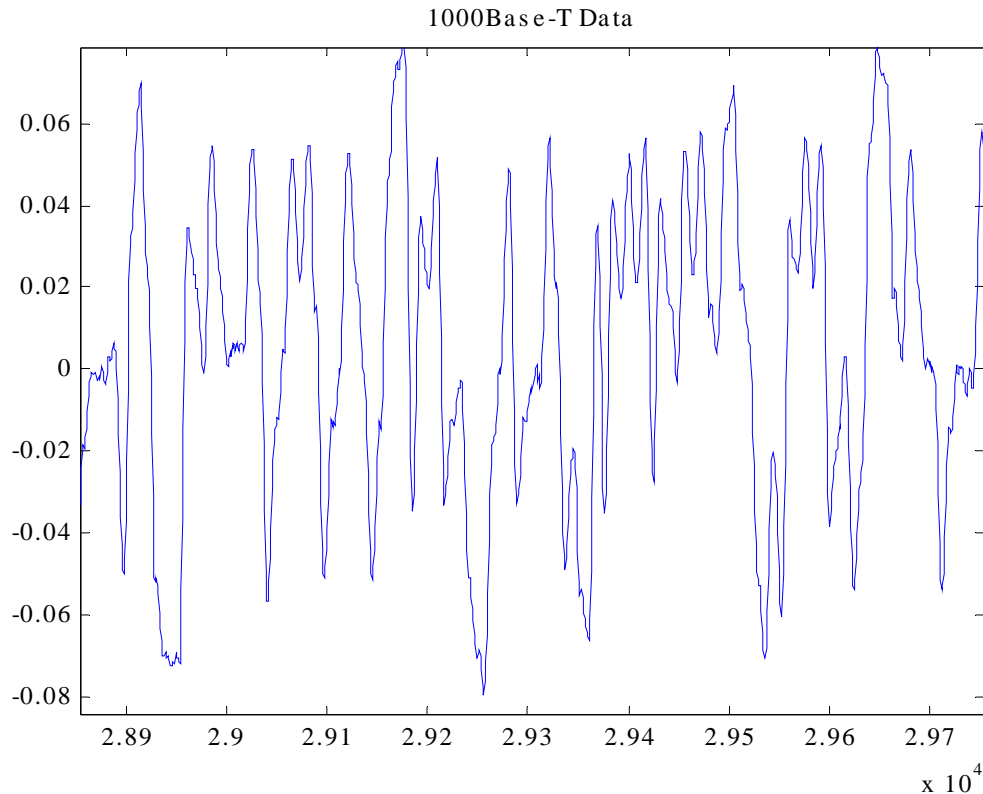
PAM-5 and Partial Response

- Partial Response acts like a digital filter
  - This is accomplished by introducing a known ISI (Inter symbol Interference)

- Digital filter is applied to transmitted PAM5 symbol stream

$$F(z) = \tfrac{3}{4}(z_n) + \tfrac{1}{4}(z_{n-1})$$

  - Where z_n is the current symbol, and z_{n-1} is the previous

- This Equation yields up to 17 different discrete voltage levels
  - In 1/8 V increments

PAM-5 and Partial Response


1000Base-T Data

- An example of the 17 possible discrete voltage levels created by the Partial Response filter

PMA Sub functions

- There are six PMA sublayer functions, starting with PMA reset, followed by 5 other simultaneous operating functions that make this possible

- Six functions:
  - PMA Reset   (40.4.2.1)
  - PMA Transmit   (40.4.2.2)
  - PMA Receive   (40.4.2.3)
  - PMA PHY Control   (40.4.2.4)
  - Link Monitor   (40.4.2.5)
  - Clock Recovery   (40.4.2.6)

Figure 40–13 — PMA reference diagram
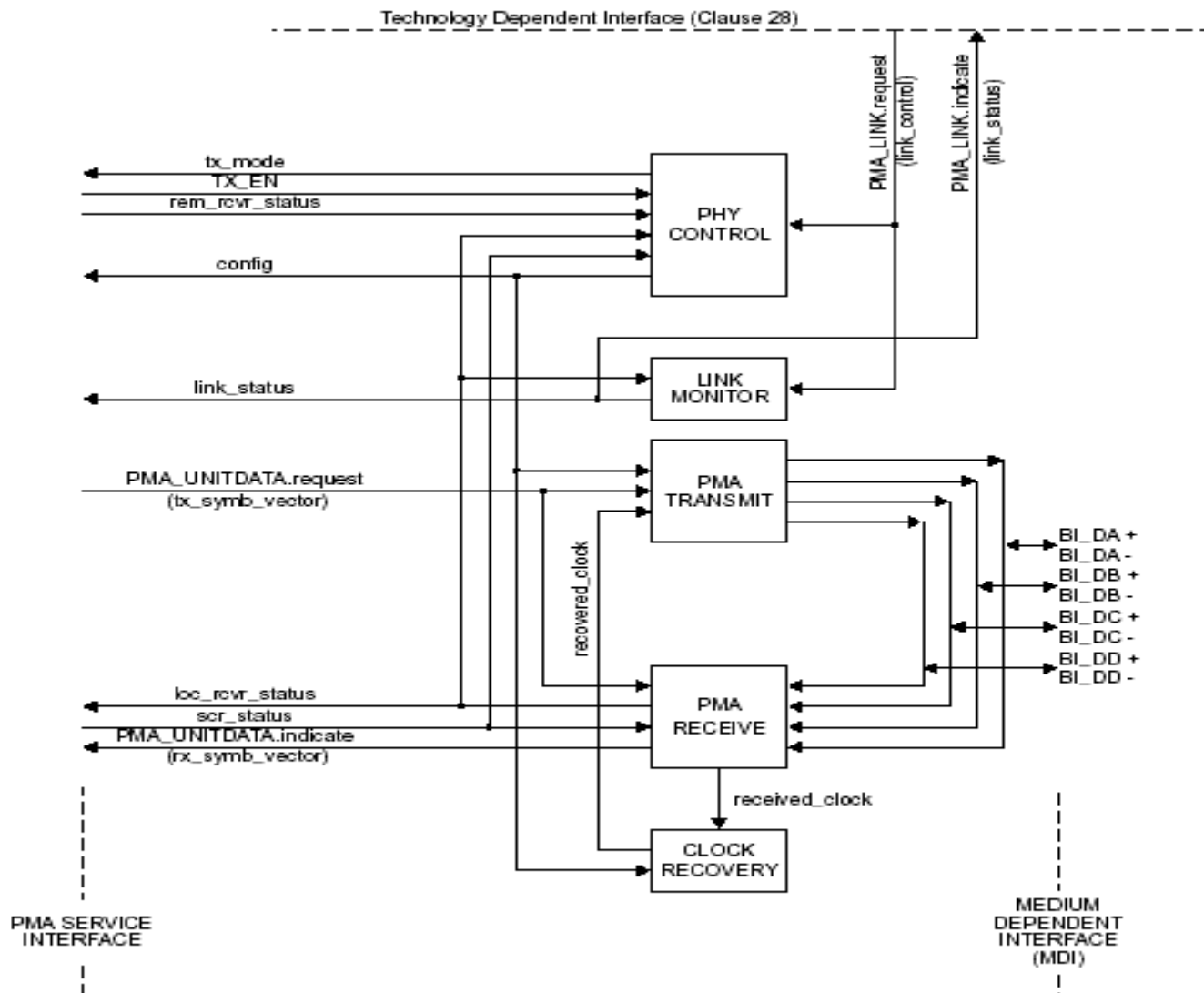
NOTE The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

UNIVERSITY of NEW HAMPSHIRE
INTEROPERABILITY LABORATORY

1000Base-T PMA

PMA Function: PMA Reset

- Initialization
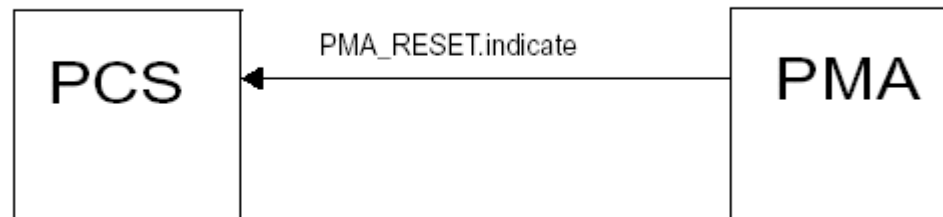 - What does it do?
  - What makes it happen?

PMA Function: PMA Reset

- Initializes the start of the other 5 simultaneous operating functions

- Used for control to restart the 5 functions including the clock recovery

PMA Function: PMA Reset

- PMA Reset is executed when one of these occurs
  - Power on
  - A request from the management entity
    - PMA Reset sets PCS_RESET=ON while one or both of the above conditions are true
    - PCS_RESET.Indicate can take one of two states, TRUE or FALSE. Where Reset is enabled when TRUE, and visa-versa

```
+---------+        PMA_RESET.indicate        +---------+
|         |  <-------------------------------|         |
|   PCS   |                                  |   PMA   |
|         |                                  |         |
+---------+                                  +---------+
```
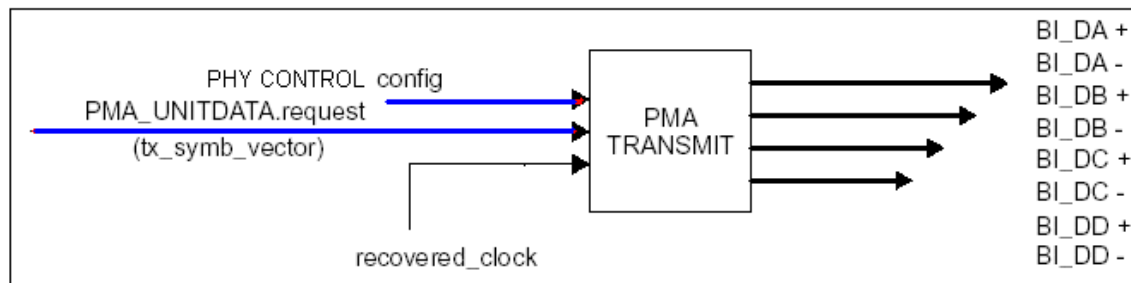
PMA Function: PMA Transmit

- The Transmit function characteristics are composed of:
  - Transmitters
  - Continuous MDI Transmitting
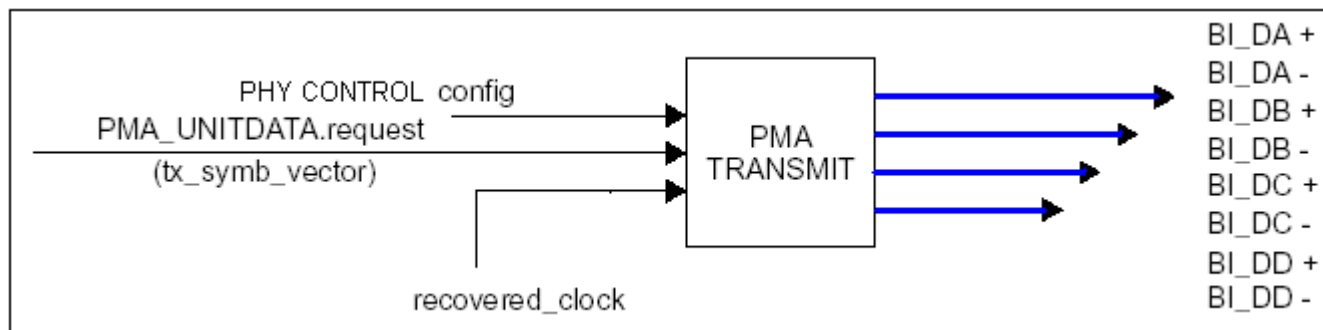 - Transmit clock
  - Jitter Conformance

PMA Function: PMA Transmit

- **During Transmission,**
    - PMA_UNITDATA.request conveys to the PMA using tx_symb_vector the value of the symbols to be sent over each of the 4 transmit pairs
    - The tx_symb_vector parameter takes the following from:
        - SYMB_4D (a vector of 4 quinary symbols, one for each pair)
    - Upon receipt of this primitive the PMA transmits on to the MDI the signals corresponding to the quinary signals received
    - PHY CONTROL Config can consist of:
    - Tx_mode= SEND_N   (Normal GMII Data stream, Control information, or idle)
        SEND_I   (Transmit of Idle code group)
        SEND_Z   (Transmit of Zero code group)

PMA Function: PMA Transmit

- Uses four synchronous transmitters to generate the PAM5 signals on each of the four pairs, BI_DA, BI_DB, BI_DC, and BI_DD
  - The Signals generated by the PMA Transmit also fit the PAM5 specifications for conformance with the MDI

PMA Function: PMA Transmit

- The four transmitters shall be driven by the same transmit clock:

  – TX_TCLK

  – The TX_TCLK, known as the transmit clock is the reference clock for the MASTER. This is later discussed as a source for Jitter testing

PMA Function: PMA Transmit

- Conforms to Jitter specifications with respect to the two conditions, Master/Slave

- When PMA_CONFIG indicates MASTER mode, the PMA Transmit Function will source the TX_TCLK from a <u>Local Clock Source</u>

- When PMA_CONFIG indicates SLAVE mode, the PMA Transmit Function will source the TX_TCLK from the <u>Recovered Clock</u> while meeting the Jitter requirements

PMA Function: PMA Receive

- Three primary PMA Receive Characteristics are shown Below:
    - Receivers
    - Abilities
    - Sub-Functions

PMA Function: PMA Receive

- Comprises four independent receivers for quinary PAM signals on each of the four pairs
  - BI_DA, BI_DB, BI_DC, and BI_DD
- Has the ability to translate the signals received on all pairs into the PMA_UNIDATA.indicate parameter rx_symb_vector with a bit error rate less than or equal to 10^{-10}

PMA Function: PMA Receive

- Contains necessary circuitry to:
  - Detect quinary symbol sequences from the signals received at the MDI over all four receive pairs
  - Present the sequences to the PCS Receive function
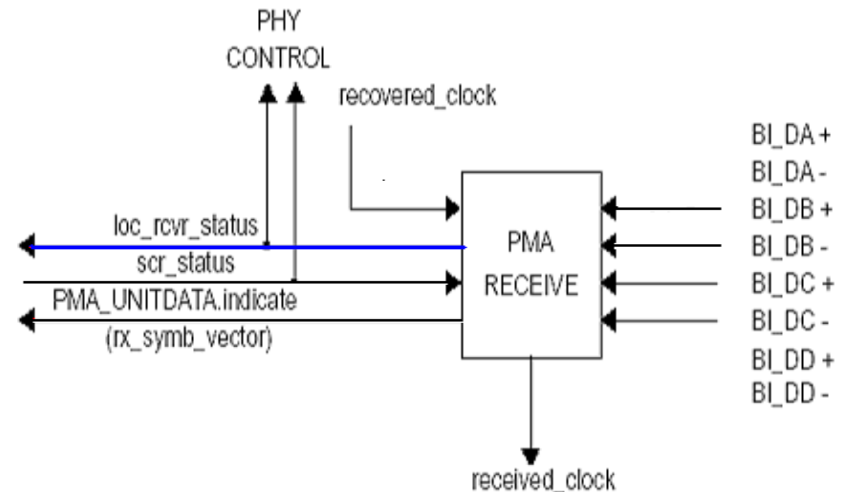
PMA Function: PMA Receive

- PMA Receive has the following sub-functions:
  - Signal Equalization, Echo and Crosstalk Cancellation, and Sequence estimation
- These Sub-Functions are used to determine the receiver performance and generate loc_rcvr_status (general status of local receiver) variables.

PMA Function: PMA Receive

Loc_rcvr_status: This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY

The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall received link is satisfactory or not.

PMA Function: PMA Receive
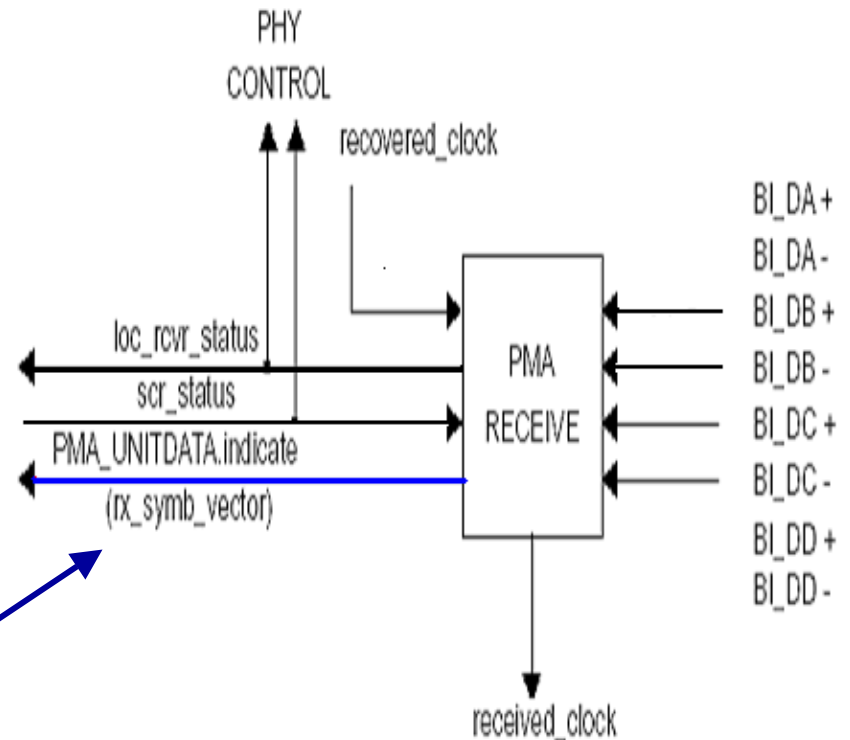
SCR_STATUS

- This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY

- The parameter scr_status conveys to the PMA Receive function that the descrambler has achieved synchronization.
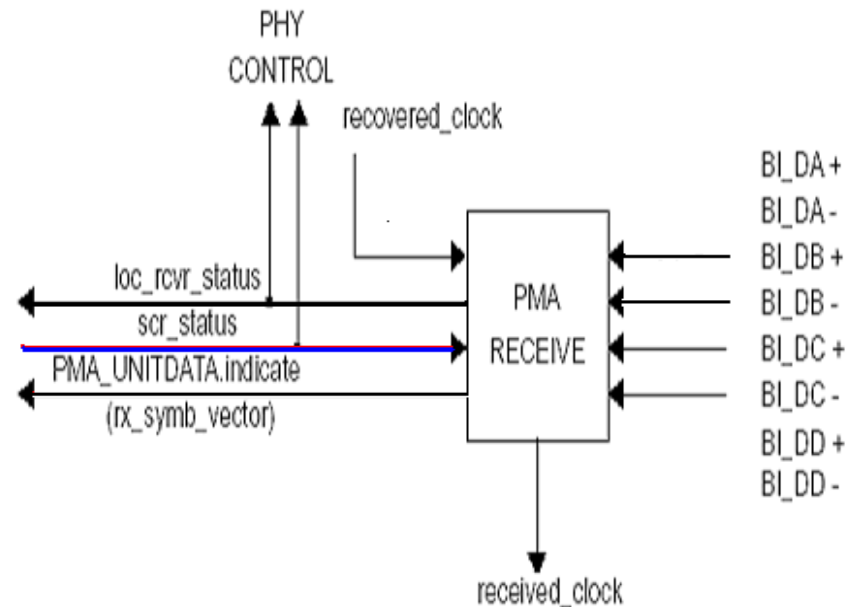
PMA Function: PMA Receive

- PMA_UNITDATA.indicate
  - Signal sent by PMA Receive
  - Is an indication that a vector of four quinary symbols is available in rx_symb_vector for the PCS

PHY CONTROL

recovered_clock

loc_rcvr_status

scr_status

PMA_UNITDATA.indicate

(rx_symb_vector)

PMA RECEIVE

BI_DA +
BI_DA –
BI_DB +
BI_DB –
BI_DC +
BI_DC –
BI_DD +
BI_DD –

received_clock

PMA Function: PHY Control

- Tasks of PMA PHY Control:
  - Generates the control actions needed to bring the PHY into the mode of operation when frames can be exchanged with the link partner.
  - Disables the Transmitter state during Auto-Negotiation
  - Forces Master and Slave control after Auto-Negotiation and starts the respective timers
  - Generates signals that control the PCS and PMA sublayer operations
  - It determines whether the PHY operates in a normal state, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode

PMA Function: PHY Control

40.4.6.1 PHY Control state diagram
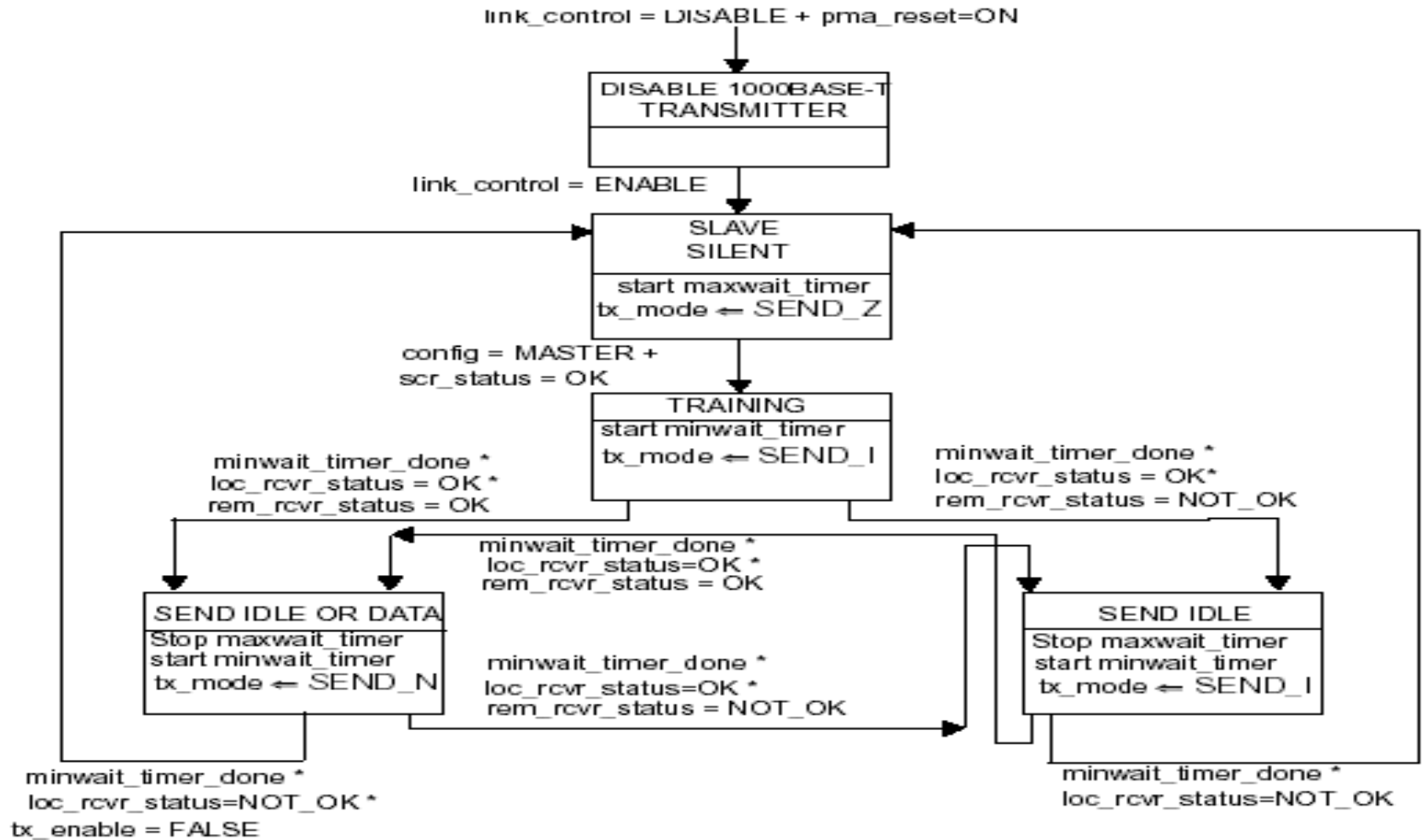
PMA Function: PHY Control

Initially (during Auto-Negotiation) the PHY Control is in:

DISABLE 1000Base-T TRANSMITTER state where all 4 transmitters are disabled.

If A-Neg asserts link_control=ENABLE, PHY Control enters SLAVE SILENT state, starts the maxwait_timer and forces the transmission of all zeros.

Note: Max Wait is defined in SLAVE mode to be 350 ± 5 ms and in MASTER mode as 750 ± 10 ms

Note: Min Wait is defined as $1 \pm .1$ us

link_control = DISABLE + pma_reset=ON

DISABLE 1000BASE-T TRANSMITTER

link_control = ENABLE

SLAVE SILENT

start maxwait_timer
tx_mode ⇐ SEND_Z
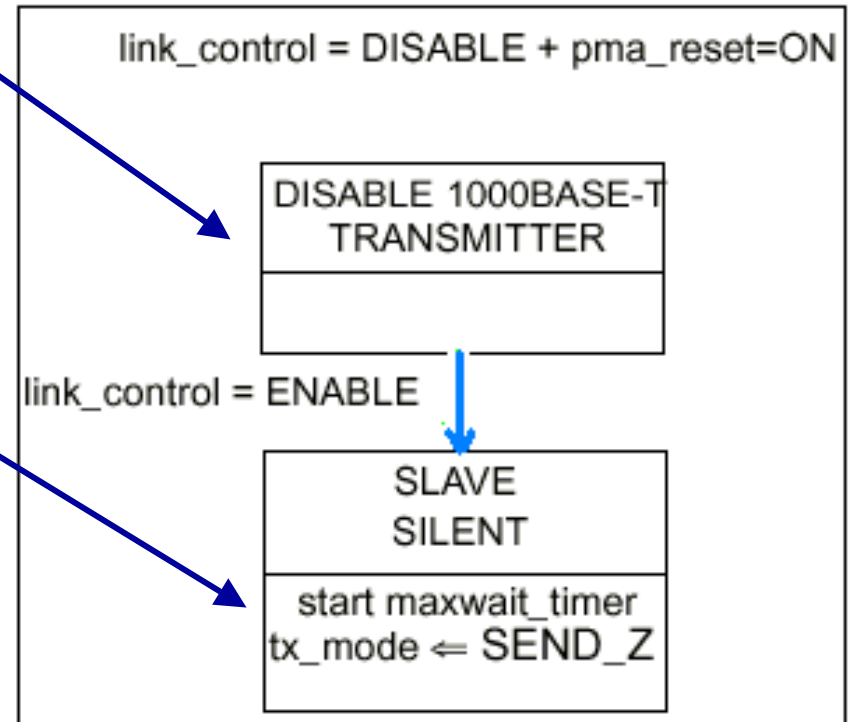
PMA Function: PHY Control
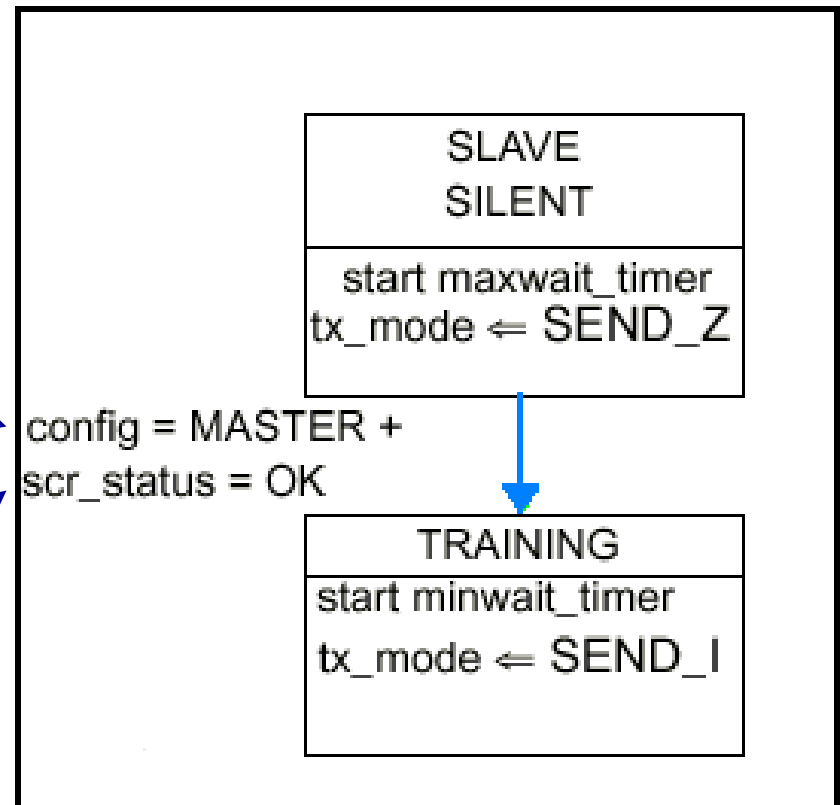
- The transition from SLAVE SILENT to the TRAINING state is determined by which mode the PHY is operating in (Master/Slave)

If Master mode, the transition is instant

If Slave mode, the SLAVE PHY Converges the Decision Feedback Equalizer (DFE), acquires timing, acquires a descrambler state, and sets scr_status=OK.

Once in this state, the minimum wait timer is started and the device is forced to transmit idle. The purpose of the training state is to converge the adaptive filter parameters

SLAVE
SILENT

start maxwait_timer
tx_mode $\Leftarrow$ SEND_Z

config = MASTER +
scr_status = OK

TRAINING
start minwait_timer
tx_mode $\Leftarrow$ SEND_I
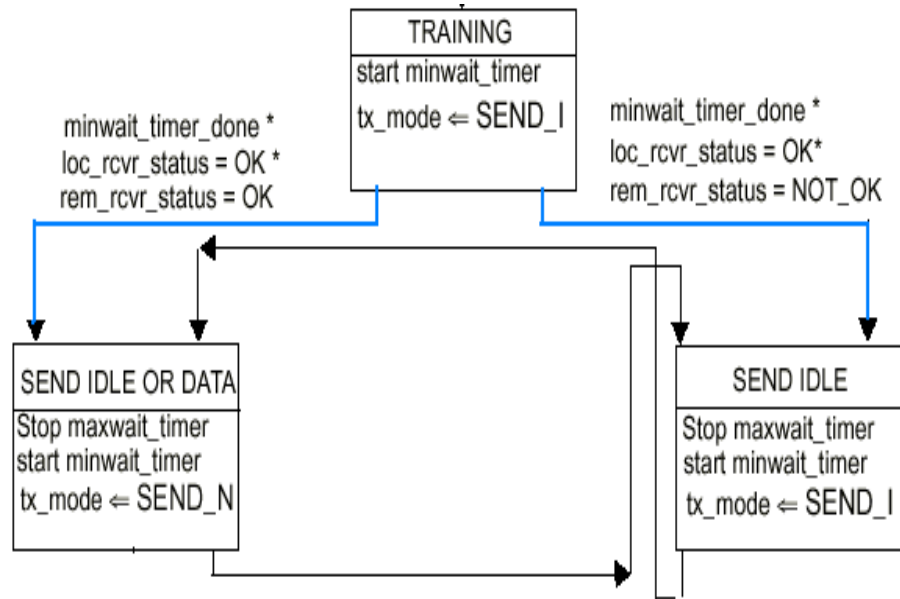
PMA Function: PHY Control

- After the TRAINING state the PHY Control transitions into either the "SEND IDLE OR DATA" or "SEND IDLE" State. The conditions that determine this move are:
  - minimum wait timer expires, status of the overall receive link(loc_rcvr_status), and the detection of a reliable remote PHY.

IF a reliable remote PHY is not detected (rem_rcvr_status=NOT_OK)
THEN the PHY control goes to the SEND IDLE state, where the Maximum wait timer is stopped, the Minimum wait timer is started, and the PHY is forced to transmit IDLE
ELSE-IF a reliable remote PHY is detected (rem_rcvr_status=OK)
THEN the PHY Control goes to the SEND IDLE OR DATA state where max wait is stopped, min wait is started, and it is granted the ability to transmit data or idle if no data is present

TRAINING
start minwait_timer
tx_mode ⇐ SEND_I

minwait_timer_done *
loc_rcvr_status = OK *
rem_rcvr_status = OK

minwait_timer_done *
loc_rcvr_status = OK*
rem_rcvr_status = NOT_OK

SEND IDLE OR DATA
Stop maxwait_timer
start minwait_timer
tx_mode ⇐ SEND_N

SEND IDLE
Stop maxwait_timer
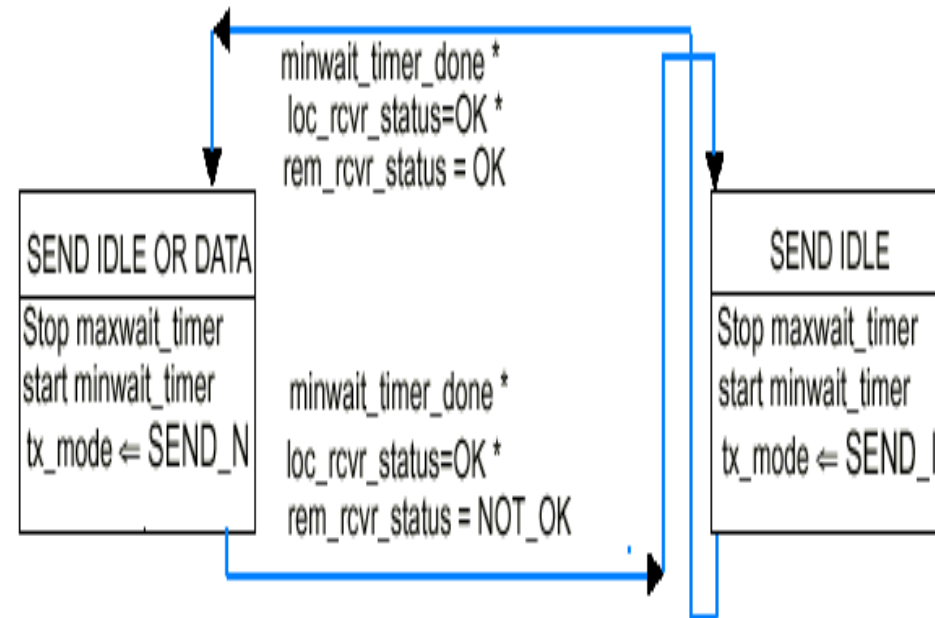start minwait_timer
tx_mode ⇐ SEND_I

PMA Function: PHY Control

- If at any point during these two states given the min wait timer is done and receive status is good:

IF in SEND IDLE OR DATA state and the PHY detects an unsatisfactory remote receiver the transmission of data will finish and the PHY control will enter the SEND IDLE state

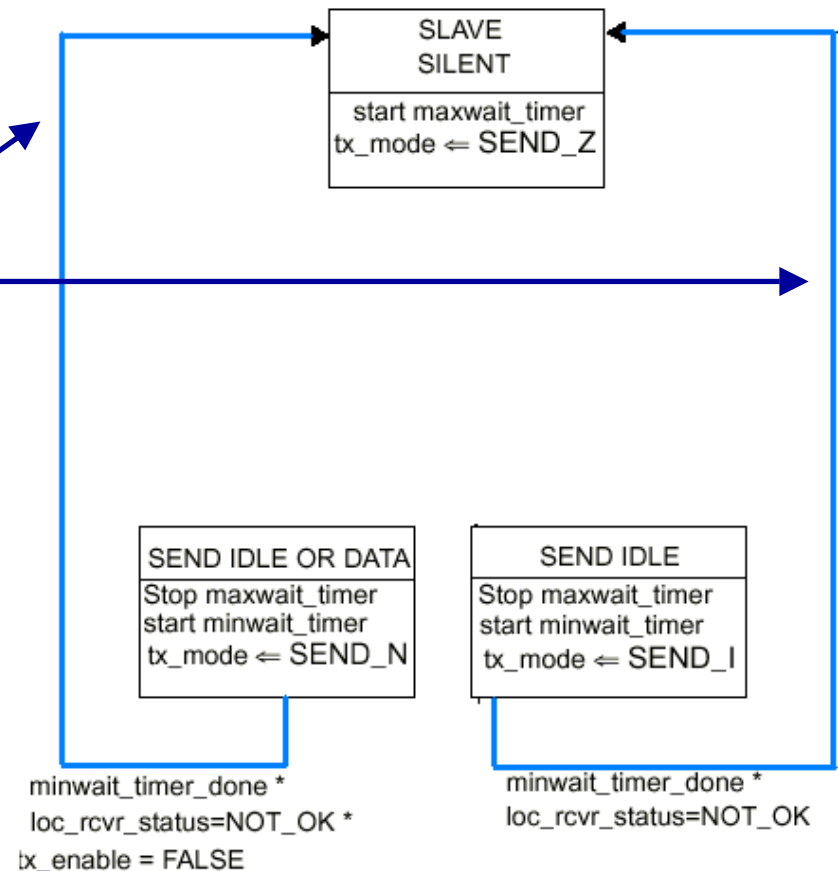**IF** in the SEND IDLE state and the PHY detects a satisfactory remote receiver PHY Control will enter the SEND IDLE or DATA state.

minwait_timer_done *
loc_rcvr_status=OK *
rem_rcvr_status = OK

SEND IDLE OR DATA

Stop maxwait_timer
start minwait_timer
tx_mode ⇐ SEND_N

minwait_timer_done *
loc_rcvr_status=OK *
rem_rcvr_status = NOT_OK

SEND IDLE

Stop maxwait_timer
start minwait_timer
tx_mode ⇐ SEND_I

PMA Function: PHY Control

At any point in the SEND IDLE or SEND IDLE or DATA state if the min wait timer expires and the local PHY receiver status becomes unstable, the PHY control is directed back to the SLAVE SILENT state after completing transmission of the current frame.

- This effectively restarts the PHY control process

SLAVE SILENT
start maxwait_timer
$tx\_mode \Leftarrow SEND\_Z$

SEND IDLE OR DATA
Stop maxwait_timer
start minwait_timer
$tx\_mode \Leftarrow SEND\_N$

SEND IDLE
Stop maxwait_timer
start minwait_timer
$tx\_mode \Leftarrow SEND\_I$

minwait_timer_done *
loc_rcvr_status=NOT_OK *
tx_enable = FALSE

minwait_timer_done *
loc_rcvr_status=NOT_OK

PMA Function: Link Monitor

- Determines the status of the underlying receive channel by communicating via the Link_status

- Auto-Negotiation sets the Link_control depending on the reception of FLPs

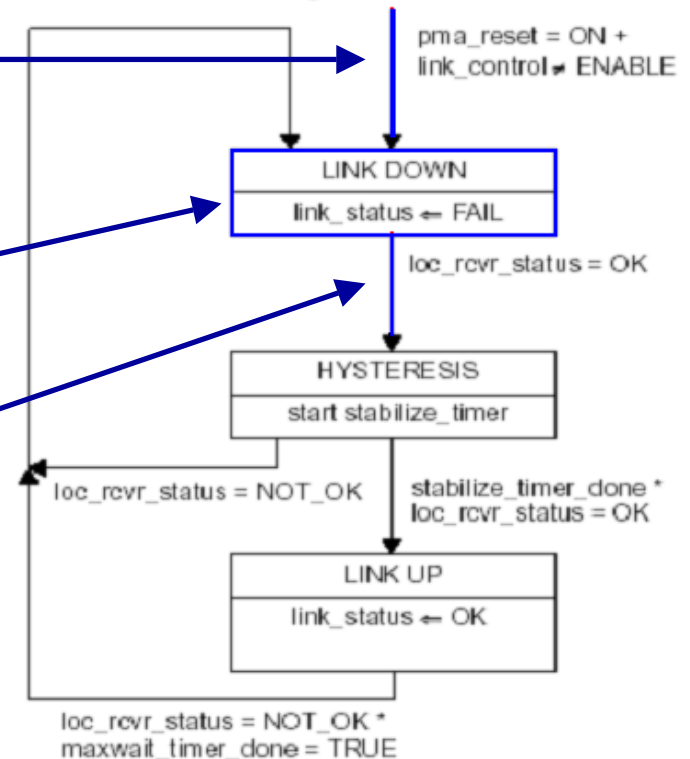- This function is better described by the following state diagram:

PMA Function: Link Monitor

While, pma_reset = ON (Reset is enabled) or link_control = disable (scan_for_carrier was able to detect FLPs and the link is down, auto-neg information is enabled with the link partner)

Then, Link_status = FAIL

Until, Loc_rcvr_status = OK, (conveys information about the status of the overall receive link, in this case if OK)

40.4.6.2 Link Monitor state diagram

pma_reset = ON +
link_control ≠ ENABLE

LINK DOWN

link_status ← FAIL

loc_rcvr_status = OK

HYSTERESIS

start stabilize_timer

loc_rcvr_status = NOT_OK

stabilize_timer_done *
loc_rcvr_status = OK

LINK UP

link_status ← OK

loc_rcvr_status = NOT_OK *
maxwait_timer_done = TRUE

PMA Function: Link Monitor

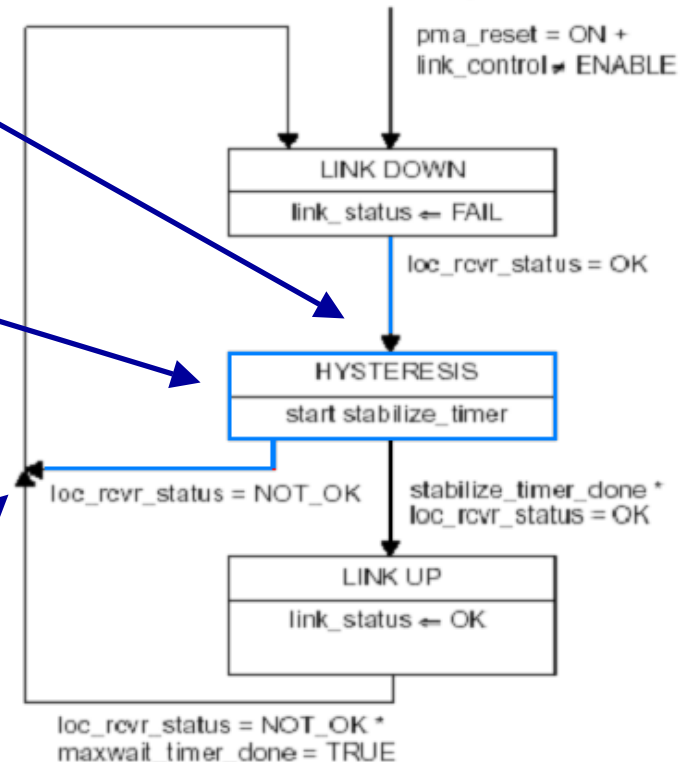**IF** Loc_rcvr_status = OK, (conveys information about the status of the overall receive link)

THEN, go to the HYSTERESIS state which means (waiting for change). Start stabilize_timer (a timer used to control the minimum time that loc_rcvr_status must be OK before a transition to Link Up can happen)

– Timer expires after 1 ± 0.1 µs

IF, Loc_rcvr_status = NOT_OK

THEN, Return and set link_status = FAIL

40.4.6.2 Link Monitor state diagram

pma_reset = ON +
link_control ≠ ENABLE

LINK DOWN

link_status ← FAIL

loc_rcvr_status = OK

HYSTERESIS

start stabilize_timer

loc_rcvr_status = NOT_OK

stabilize_timer_done *
loc_rcvr_status = OK

LINK UP

link_status ← OK

loc_rcvr_status = NOT_OK *
maxwait_timer_done = TRUE

PMA Function: Link Monitor

IF, stabilize_timer_done and loc_rcvr_status = OK (local receiver status ok and stabilize timer expires)

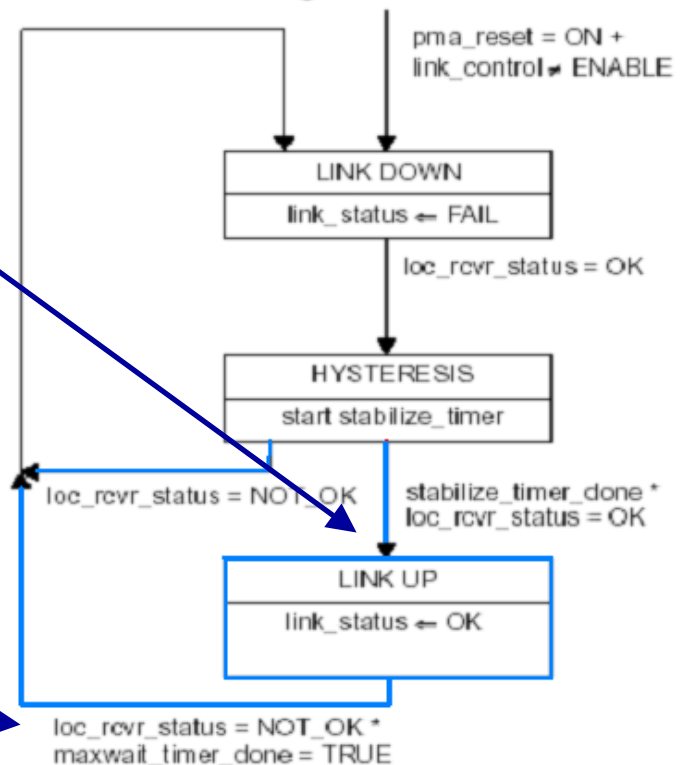THEN, proceed to LINK UP state and OK is applied Link_status

ELSE-IF, Loc_rcvr_status = NOT_OK (PHY does not see a reliable receive link)

THEN, link monitor goes back to LINK DOWN state and link_status = FAIL

When in the LINK UP state IF the local receiver becomes unstable and the max wait timer has ended

THEN link monitor returns to link down

40.4.6.2 Link Monitor state diagram

pma_reset = ON + link_control ≠ ENABLE

LINK DOWN
link_status ← FAIL

loc_rcvr_status = OK

HYSTERESIS
start stabilize_timer

loc_rcvr_status = NOT_OK

stabilize_timer_done * loc_rcvr_status = OK

LINK UP
link_status ← OK

loc_rcvr_status = NOT_OK * maxwait_timer_done = TRUE

PMA Functions: Clock Recovery

- Recovers the clock from the received stream

- Coupled to all four receive pairs

- Can provide independent clock phases for sampling signals on each pair

- Provides a suitable clock for signal sampling on each line to achieve the symbol error rate

- Used as an input variable for other PMA Functions

PMA Electrical

- PMA Electrical is broken into several parts:

  - Isolation requirements

  - Test Channel setup

  - 4 Test Modes

  - Transmitter Distortion

  - Transmitter Timing Jitter

PMA Electrical: Isolation

- Isolation Requirement:
  - The PHY shall provide electrical isolation between the port device circuit and all MDI leads and withstand the following stress tests:
    - 1500 V rms at 50 Hz to 60 Hz for 60 s
    - 2250 Vdc for 60 s
    - A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s

PMA Electrical: Test Channel

- Transmitter MASTER-SLAVE timing jitter test require a **Test Channel** to ensure the signal is measured under conditions of poor signal echo ratio constructed from 100 and 120 Ohm Cat5 cable

- Shown at right is the Test channel topology and the Test channel Cable Specifications
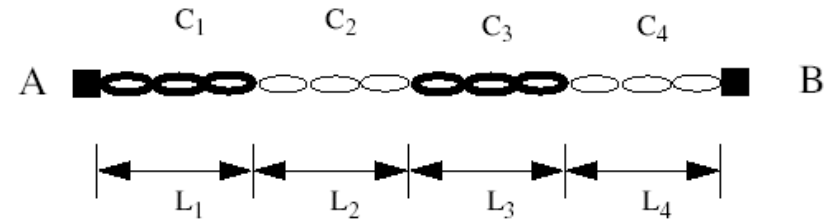
Identical for each of the four pairs.

Table 40–6—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	$L_1=1.20$	$120 \pm 5\Omega$	7.8 to 8.8 dB
2	$L_2=x$	$100 \pm 5\Omega$	10.8 to 11.8 dB
3	$L_3=1.48$	$120 \pm 5\Omega$	7.8 to 8.8 dB
4	$L_4=y$	$100 \pm 5\Omega$	10.8 to 11.8 dB

PMA Electrical: Test Modes

- There are four test modes that shall be provided by the PMA to allow testing of:
  - transmitter waveform, transmitter distortion, and transmitted jitter.
- These Test Modes can be enabled by setting bits 9.13:15 (1000Base-T Control Register)
- These Test Modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

PMA Electrical: Test Modes

- At right are the Bit assignments to access the 4 PMA Test Modes.

- These modes are enabled by setting bits 9.13:15 if the device is equipped with a GMII interface.

- These test modes should only change the data symbols provided by the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver

Table 40–7—GMII management register settings for test modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Mode
0	0	0	Normal operation
0	0	1	Test mode 1—Transmit waveform test
0	1	0	Test mode 2—Transmit jitter test in MASTER mode
0	1	1	Test mode 3—Transmit jitter test in SLAVE mode
1	0	0	Test mode 4—Transmitter distortion test
1	0	1	Reserved, operations not identified.
1	1	0	Reserved, operations not identified.
1	1	1	Reserved, operations not identified.

PMA Electrical: Test Mode 1

- In test mode 1 the PHY shall transmit the following sequence on all four transmitters continually from a 125MHz clock in MASTER timing mode:
  - {{+2 followed by 127 0 symbols}, {−2 followed by 127 0 symbols},{+1 followed by 127 0 symbols},{−1 followed by 127 0 symbols}, {128 +2 symbols, 128 −2 symbols, 128 +2 symbols, 128 −2 symbols},{1024 0 symbols}}

PMA Electrical: Test Mode 1

- At right is the typical wave form shape with the 11 letters representing points that are used for further reference:
  - A = +2s ; B = -2s ; C = +1s
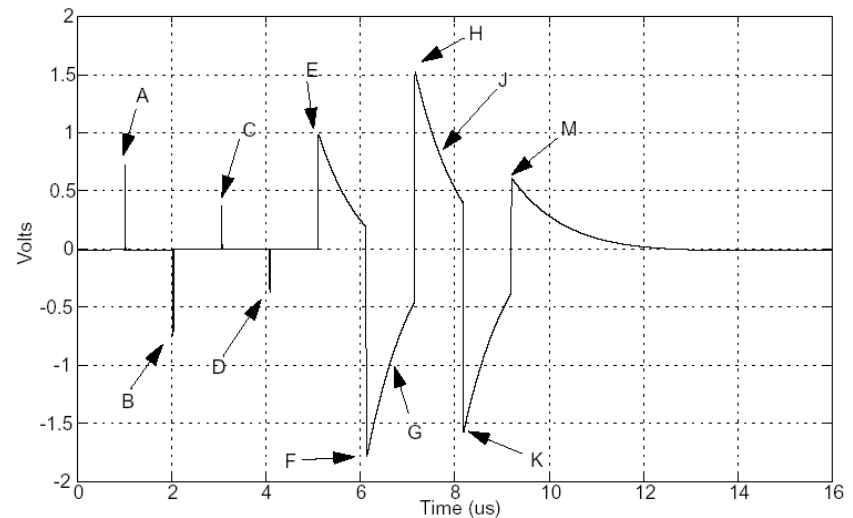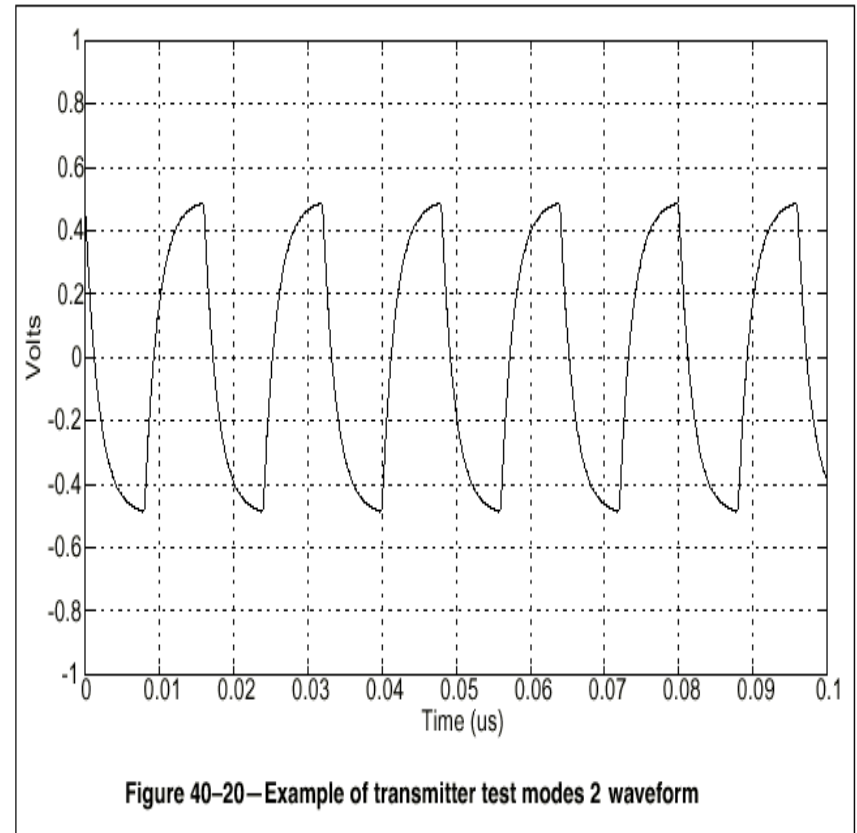 - D = -1s; ...
  - (where s is Symbol)

Figure 40–19—Example of transmitter test mode 1 waveform (1 cycle)
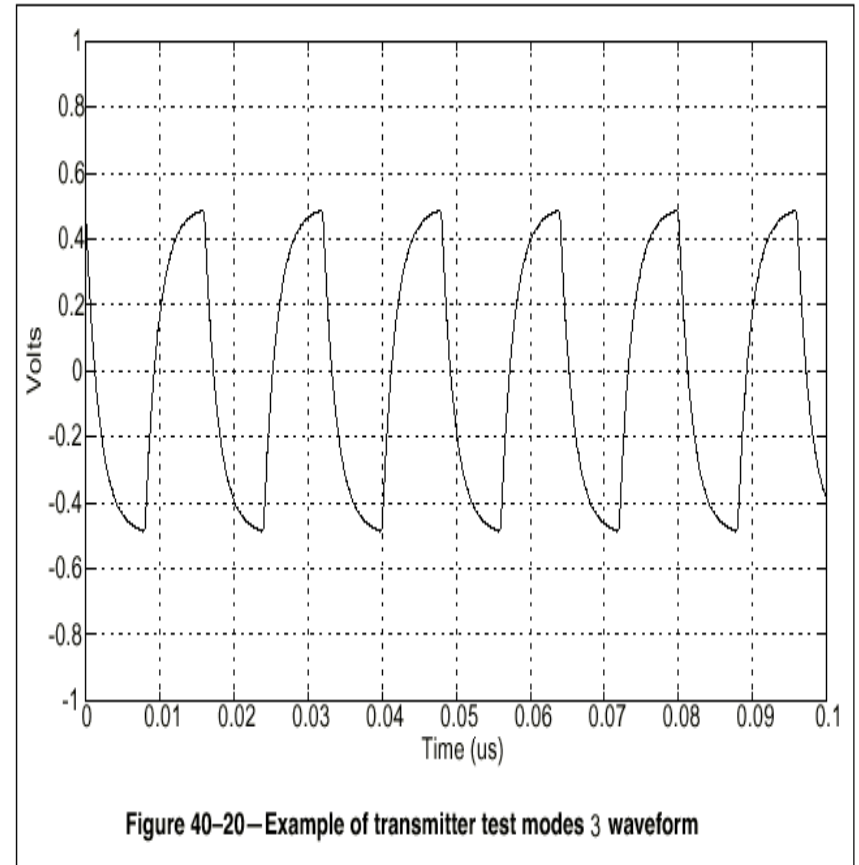
PMA Electrical: Test Mode 2

- The PHY transmits a data symbol sequence of {+2,-2} repeatedly on all channels with a signal clock of 125 Mhz in **MASTER** timing mode.

- At right is the typical Test mode 2 waveform


Figure 40–20—Example of transmitter test modes 2 waveform

PMA Electrical: Test Mode 3

- The PHY transmits a data symbol sequence of {+2,-2} repeatedly on all channels with a signal clock of 125 Mhz in **SLAVE** timing mode.

- At right is the typical Test mode 3 waveform

  – Note: This is the same wave from as Test Mode 2 because of the identical symbol sequence

Figure 40–20—Example of transmitter test modes 3 waveform

PMA Electrical: Test Mode 4

- When Test mode 4 is enabled, the PHY transmits a sequence of symbols generated by the following scrambler polynomial:
  - $g_{s1} = 1 + x^9 + x^{11}$

- The 11-Bit Linear Feedback Shift Register used to generate this sequence is shown at right. This shift register is loaded with an initial "Symbol Map" at start up.
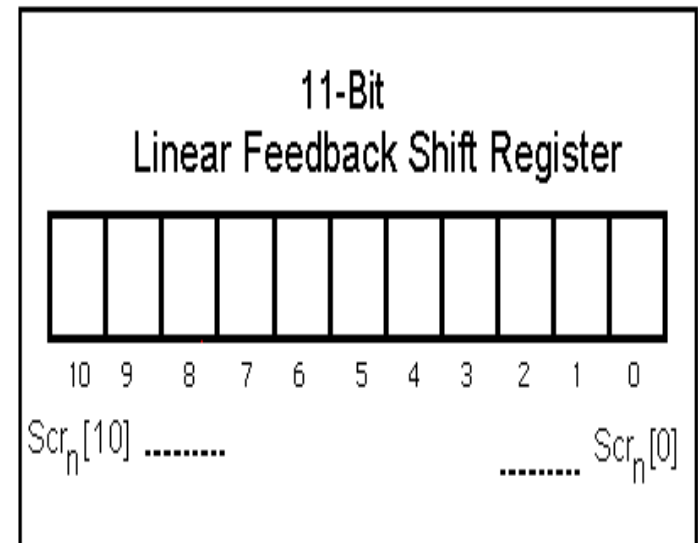
PMA Electrical: Test Mode 4

- The Linear Feedback Shift Register is updated once every symbol interval
  - 8 ns, or 1/125MHz

- At every interval the shift register is advanced one bit to the left and generates a new bit as shown:
  - $Scr_n[0] \leftarrow Scr_n[10] \oplus Scr_n[8]$
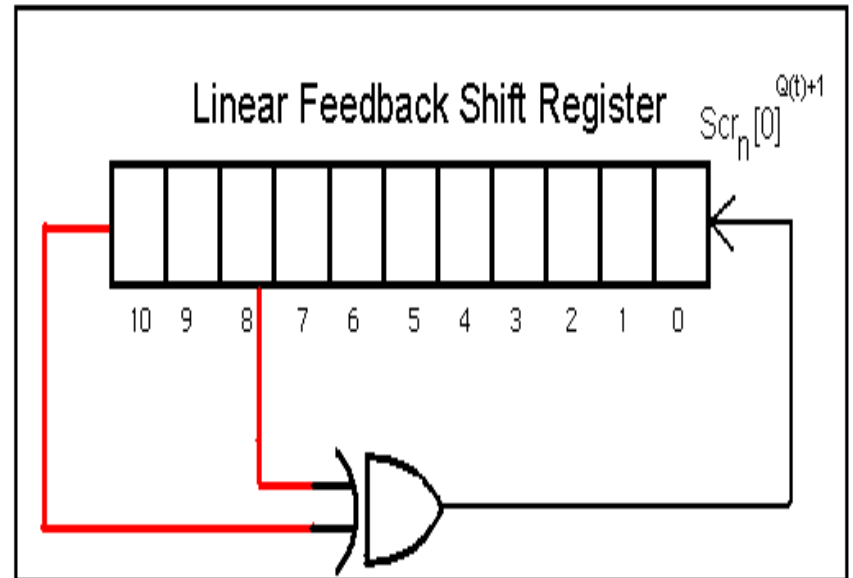
PMA Electrical: Test Mode 4

- Three Bit sequences ($x0_n$, $x1_n$, and $x2_n$) are made form the equations shown at upper right and the respective bits held in the 11-bit Shift Register.

$$x0_n = Scr_n[0]$$

$$x1_n = Scr_n[1] \wedge Scr_n[4]$$

$$x2_n = Scr_n[2] \wedge Scr_n[4]$$

- These three bit sequences are then matched to a symbol map that equates the three bit sequence to a quinary symbol as shown at lower right:

x2n	x1n	x0n	quinary symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	−1
1	0	0	0
1	0	1	1
1	1	0	−2
1	1	1	−1

PMA Electrical: Test Mode 4

- Shown below is the typical test mode 4 output. What would be normally 5 levels is shown as a pseudo random 17 level waveform after partial response is applied.
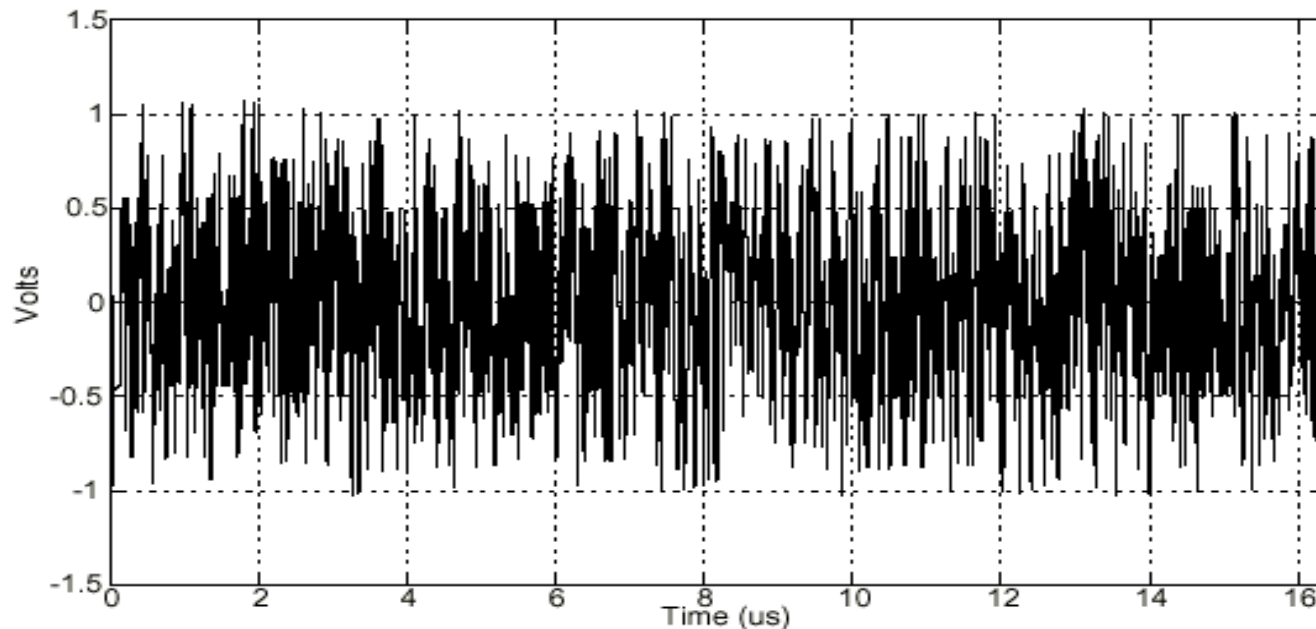
PMA Electrical: Transmitter Distortion

- Transmitter Distortion is a measured with the device in Test Mode 4 by observing the differential signal output at the MDI on each pair.

- The peak distortion shall not exceed 10 mV (as defined by 802.3).

- Peak Distortion is determined by comparing the received sequence with the ideal waveform.

PMA Electrical: Transmitter Timing Jitter

- Jitter is the difference between the time that an event was expected to occur and the time that the event actually occurred. In the context of a digital communications link, jitter is the offset between the expected position of a signal transition and the actual position of the transition. The magnitude of these offsets must be limited in order to limit the chances of an error on the link.

1000Base-T PMA

PMA Electrical: Transmitter Timing Jitter

- Jitter is the measure of the peak-to-peak deviations in time of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of the transmit clock.

- The transmit clock edge is defined as the edge of the test clock with matching polarity and time that generates the zero-crossing transitions that are measured.

In Summary

- PMA is primarily used to serialize and de-serialize the incoming data stream

- Acts as digital filter by applying partial response

- Converts the 5 level encoding known as PAM-5 into 5 discrete voltage levels

- PMA is also responsible for many of the Transmitter electrical characteristics such as Timing Jitter and Distortion

Additional resources

- IEEE 802.3-2002 Standard

- 1000Base-T PMA Test Suite

- 100Base-TX PMD Test Suite

- Beckwith's Brain/Plante's Brain

- Gary Pressler's Presentations